PULSED AND CW DOUBLE-DRIFT SILICON IMPATTS

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ABSTRACT

The properties of double-drift Si IMPATTs designed for both pulsed and CW operation at frequencies between 8 and 18 GHz are discussed. Peak pulse powers greater than 18 watts at 10 GHz and 13.5 watts at 16.5 GHz were obtained for 800 nsec pulses at a 25% duty cycle with the junction temperature rise limited to 200°C. For a similar temperature rise a CW power of 3.4 watts at 11.5 GHz was achieved. Conversion efficiencies were between 10.5 and 13.7%.

Introduction

The double-drift P^+PNN^+ IMPATT structure has been shown to offer significant advantages in power generating capability and efficiency over the extensivelystudied flat-profile P^+NN^+ structure.[1,2,3] In particular Seidel, et al[1] obtained 0.75 watts at 50 GHz with 11% efficiency at a junction temperature of 250°C. The superiority of double-drift over P^+NN^+ devices appears to stem from an approximately 1/3 lower capacitance per unit area and a smaller ratio of avalanche region to drift region voltage. The smaller capacitance per unit area allows larger area devices to be easily resonated while the lower avalanche/drift voltage ratio leads directly to higher efficiencies.

The active regions of the silicon devices whose performance is considered in this paper were formed by the successive silane growth of n and p epitaxial layers on low-resistivity arsenic substrates. The choice of n and p layer impurity concentrations was made on the basis of a design philosophy similar to that of Lekholm and Mayr[4] which attempts to equalize the electron and hole transit times in their respective drift regions. The most significant difference in the structure of layers designed for pulsed and CW operation was the presence of considerably more undepleted p and n material in the pulsed case.

All devices were fabricated by an integral plated silver heatsink process. CW diodes utilized either one or two round mesas in standard ceramic packages. Pulsed diodes had annular shaped mesas with annulus widths of approximately 75 microns. These mesa geometries represent a compromise between the desire to minimize thermal impedance, insure avalanche uniformity and minimize fabrication difficulties.

Pulsed Performance

Pulsed devices designed for operation centered at 10, 14, and 16.5 GHz were operated as oscillators in a simple fixed coaxial cavity. The proper load resistance was obtained in each case by selecting an appropriate single step transformer. The load resistance presented to the package was found to be approximately proportional to current density. Due to higher operating currents the optimum load resistance for pulsed operation was from 2 to 4 times greater and the negative Q lower than for CW operation.

The pulsed diodes were biased by adding a voltage pulse to a fixed d.c. bias voltage slightly less than the diode's breakdown voltage. Excellent pulse spectrum quality with side nodes greater than 40 dB below the maximum could easily be achieved by using a high output impedance transistor pulse amplifier which allowed for a controlled increase in the bias current during the pulse.[5] The slight increase in the current readily compensated for the thermally induced decrease in the frequency as the diode temperature increased.

The c.w. and pulsed microwave characteristics typical of a large number of diodes from several epitaxial growth runs are summarized below:

Center Frequency (GHz)	10	14	16.5
Efficiency (%)	12	8.2	11.5
Peak Power (watts)	14	20	11
Breakdown Voltage	115	93	77
Bias Voltage	148	128	100
Bias Current (A)	0.81	1.9	0.9
Junction Capacitance (pF)	1.25	1.2	0.8
Average Temperature Rise (°C)	<175	<175	<175
Thermal Impedance (°C/W)	6.5	7	8.5
Pulse Width (nsec)	800	125	800
Duty Cycle (%)	25	10	25

The highest peak power obtained with the junction rise, ΔT_j, limited to 200°C was 18 watts at 10 GHz for a duty cycle of 25%. Curves for peak output power efficiency, and temperature rise versus bias current for such a device are illustrated in Fig. 1. Figure 2 illustrates the decrease in peak pulse power obtainable from a typical 10 GHz device as the pulse width is increased with the duty cycle held at 25% and ΔT_j limited to 200°C. The highest efficiency observed was 13.7% at 16.5 GHz with a peak output power of 11.2 watts and ΔT_j <150°C.

CW Performance

Devices were also designed for CW operation centered in the 10.7 to 11.7 GHz frequency band. Their operating behavior was similar to that of the pulsed devices except that high effeciency was achieved at lower current densities of 500 to 750 A/cm^2.

A typical performance of both one and two mesa devices is summarized below:

	SINGLE MESA	DOUBLE MESA
Efficiency (%)	11	10.5
Power Output (watts)	1.75	2.8
Breakdown Voltage	98	98
Bias Voltage	122	122
Bias Current (mA)	130	220
Junction Capacitance at V_b (pF)	0.4	0.8
Junction Temperature Rise (°C)	<200	<200
Thermal Impedance (°C/W)	14	8

The variation of output power, efficiency and temperature rise versus bias current for the best single and double mesa diodes is illustrated in Fig. 3. The double mesa diode delivered 4.6 watts with 12.8% efficiency at a ΔT_j <250°C. At the same temperature rise the single mesa diode delivered 2.8 watts with 13.2% efficiency.

In addition to a power and efficiency superiority over flat-profile single-drift Si IMPATTs, double-drift devices were observed to be capable of useful power generation over about 20% larger frequency range. For example, greater than 2 watts could be obtained from 8.2 to 14 GHz from a double-mesa diode. This large useful bandwidth is beleived to be an intrinsic property of the double-drift structure.

Conclusion

The high power-generating capabilities of double-drift Si IMPATTs in the 8 to 18 GHz range has been demonstrated for both pulsed and CW operation. The CW efficiency of 12.8% obtained at a ΔT_j <200°C is the highest reported for any silicon IMPATT under these conditions.

References

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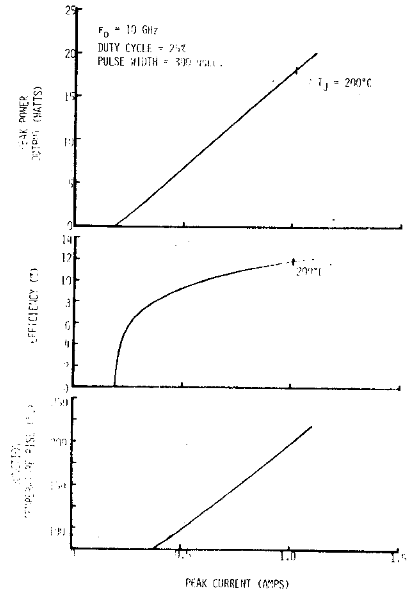

Fig. 1. Peak output power, efficiency, and junction temperature rise versus pulse current for best 10 GHz device.

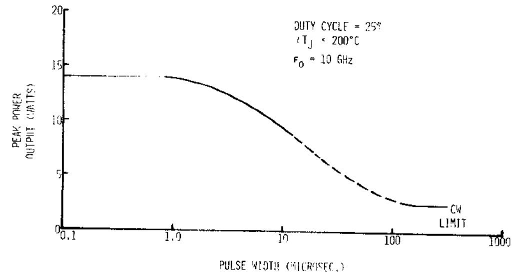

Fig. 2. Peak output power of typical diode versus pulse width for ΔT_j <200°C and 25% duty cycle.

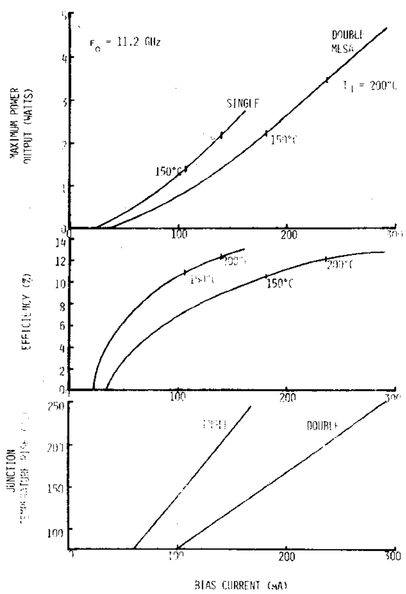

Fig. 3. Output power, efficiency and junction temperature rise versus bias current for best single and double mesa CW diodes.